done on the falling edge of the F pulse (i.e. signal F is fed into the OR-gate whose output is connected to INC). Would it be possible to use signal E instead of signal F here? Why or why not?

5a. Note that the LOAD IMMEDIATE instruction of Processor I has the annoying limitation that the constant which is loaded, namely $Z$, has the top 3 bits set to zero. What block of code would you use to get the constant $-1$ in two's complement form (all bits set to one) into the AC register?

5b. Write a block of code starting at location 0 for Processor I which will add a two's complement integer in location 100 (decimal) to a two's complement integer in location 101 (decimal) and

   i. if the result is greater than or equal to 0 jump to location 40 (decimal) and continue.

   ii. if the result is negative store the result in location 102 (decimal) and halt.