2. A circuit is to accept a 4-bit (unsigned) integer \( b_3b_2b_1b_0 \) (representing the numbers from 0 to 15) and generate one output \( c_0 \). The output \( c_0 \) is to be logical 1 if the input is evenly divisible by 2, 3, or 5, otherwise it should be logical 0 (note: zero is evenly divisible by every non-zero number).

2a. Synthesize a combinatorial circuit which will implement the above specification as efficiently as possible using only NAND gates and INVERTERS.

2b. Could you reduce the number of logic gates you used in 5a. if you were told in addition that 0001, 0011, and 1011 are “don’t care” inputs? If so, show your improved circuit; if not, explain why not.

3. Synthesize a synchronous sequential circuit which implements the finite state machine at right in as efficient a manner as possible. Use two \( JK \)-flip-flops and label the states as on the directed graph. Note that there is one unused state and a Mealy-type output.

4a. What is the difference between core memory and static ram? Discuss the advantages and disadvantages of both.

4b. In the circuitry for Processor I note that the normal incrementation of the PC register after a fetch (and before the next fetch) is