1. Which Mips instructions cause a delay slot?
   A. la  <--- not the same as lw or sw
   B. div  <--- partial credit because div macro has a branch
   C. bne
   D. nop

2. The last stage of the Mips 5-stage pipeline is
   A. Memory Access
   B. Write Back
   C. Instruction Execute
   D. Next Decode

3. In our Mips pipeline examples, the ALU has
   A. one input and two outputs
   B. two inputs and two outputs
   C. one input and one output
   D. two inputs and one output  <--- as described in lecture

4. When optimizing an assembly language program,
   A. apply optimization techniques as early as possible.
   B. avoid the use of shift and logical instructions.
   C. get the program working correctly before optimizing.
   D. always fill a branch delay slot with a no-op instruction.
   You should actually try to put a useful operation in the delay slot for maximum optimization. Keep the CPU busy.

5. Given a well written Mips program, you start it running with the command below. At the start of the main function, what will the value in register $a0 be?

   \$ spim -f myprog.s 2 1 test
   1 2 3 4  \$a0 = 4, the argument count.

6. The Mips lui instruction loads an immediate value into the upper halfword of a destination register. lui $t,i has this operation $t = i<<16.
   Given all that, what is the value in $t3 after the following commands?

   lui $t1, 1023
   and $t2, $t1, 0xFFFFFFFFF
   srl $t3, $t2, 4

   4,190,208 or 0x003FF000 or 000000000011111111100000000000
   partial credit was given if you showed your work.

7. What is the answer to homework question #20? Circle one.  A    B
   See next page.

8. Mips has a subtract command sub, where sub $d,$s,$t means $d = $s - $t.
   Sub is used as the pseudo-instruction for the command neg, which is used to get the negative of a number. Fill in the two blanks below to define the neg pseudo-instruction.

   neg Rd, Rs  pseudo-instruction: sub Rd, 0, Rs

   Subtract Rs from zero, and Rs becomes negative Rs.
I found some documentation for this question at several places online, including the PIC32 reference manual at the link below.


PIC32MX Family Reference Manual
DS61113C-page 2-62
Preliminary
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2.15.3.2 Branch Delays and the Branch Delay Slot
All branches have an architectural delay of one instruction. The instruction immediately following a branch is said to be in the branch delay slot. If a branch or jump instruction is placed in the branch delay slot, the operation of both instructions is undefined.

Conclusion
There are some unsafe instructions that can be placed in a branch delay slot. Question 7 will be thrown out of this quiz, but the knowledge gained by this clarification should not be ignored.